CLAIMS AS AMENDED

The claims as amended appear below. All claims are reproduced for convenience.

1. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising compounds of gallium and oxygen and at least one rare earth element;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

2. (Amended) The transistor of claim 1 wherein said first layer forms an atomically abrupt interface with said upper surface.

3. (Amended) The transistor of claim 1 wherein said gate insulator structure is composed of at least three layers, including a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element.

4. (Amended) The transistor of claim 3 wherein said gate insulator structure further comprises at a third layer containing gallium and oxygen.

5. (Amended) The transistor of claim 1 said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

6. (Amended) The transistor of claim 1 wherein said gate insulator structure has a thickness of 20-300 angstroms.

7. (Amended) The transistor of claim 1 wherein said first layer forms an interface with said upper surface that extend less than four atomic layers in depth of structural interface modulation.

8. (Amended) The transistor of claim 1 wherein said first layer and said gate insulator structure protects said upper surface.

9. (Amended) The transistor of claim 1 wherein said gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at 700°C.

10. (Amended) The transistor of claim 1 wherein said source and drain ion implants provide one of an n-channel or p-channel.

11. (Amended) The transistor of claim 1 wherein said source and drain ion implants comprise at least one of Be/F and C/F.

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12. (Amended) The transistor of claim 1 wherein said upper surface comprises GaAs.

13. (Amended) The transistor of claim 1 wherein said upper surface comprises $In_xGa_{1-x}As$.

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14. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

gate insulator structure on said upper surface, said gate insulator structure comprising a first layer, a second layer, and a third layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer substantially comprising compounds of gallium and oxygen and at least one rare earth element such that the normalized relative composition of at least one of gallium, oxygen, and said at least one rare earth element in said second layer varies in a monotonic manner as a function of depth within said second insulating layer;

said third layer above said second layer, said third layer substantially comprising gallium oxygen and at least one rare earth element, said third layer being insulating;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

15. (Amended) The transistor of claim 14 wherein said first layer forms an atomically abrupt interface with said upper surface.

16. (Amended) The transistor of claim 14 wherein the gate insulator structure comprises a varying layer that substantially comprises gallium, oxygen, and at least one rare-earth element in which relative concentration of at least one of gallium, oxygen, and said at least one rare earth in said varying layer monotonically vary with depth in said layer.

17. (Amended) The transistor of claim 14 wherein said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

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18. (Amended) The transistor of claim 14 wherein the gate insulator structure has a thickness of 20-300 angstroms.

19. (Amended) The transistor of claim 14 wherein said first layer forms an interface with the compound semiconductor wafer structure that extend less than four atomic layers in depth of modulation of said interface.

20. (Amended) The transistor of claim 14 wherein said first layer and said gate insulator structure protects said upper surface.

21. (Amended) The transistor of claim 14 wherein said gate electrode comprises a metal which is stable in presence of the top layer of the gate insulator structure at 700°C.

22. (Amended) The transistor of claim 14 wherein said source and drain ion implants define an n-channel.

23. (Amended) The transistor of claim 14 wherein said source and drain ion implants comprise and Be/F and C/F, and define a p-channel.

24. (Amended) The transistor of claim 14 wherein said upper surface comprises GaAs.

25. (Amended) The transistor of claim 14 wherein said upper surface comprises $In_xGa_{1-x}As$.

26. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure positioned on said upper surface, said multilayer gate insulator structure substantially comprising alternating layers each of which comprises gallium,

oxygen, and at least one rare-earth element;

a gate electrode positioned on said multilayer gate insulator structure;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

and dielectric spacers positioned on sidewalls of said gate electrode.

27-35. - Canceled by this amendment.

36. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, In_yGa_{1-y}As, InP, or $In_zGa_{1-z}P$ layer, said layer being positioned on said upper surface;

a substrate on which resides said compound semiconductor wafer structure; and

wherein said substrate includes a InP based semiconductor wafer.

37. (Amended) A complementary metal-oxide compound semiconductor integrated circuit comprising the transistor of claim 1, 13, or 26 integrated together with similar and complementary transistor devices to form said complementary metal-oxide compound semiconductor integrated circuit.

38. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface;

a gate electrode positioned on said upper surface;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer;

wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$; and

and wherein said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit.

39. An enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

a gate electrode positioned on said gate insulator structure.

40. The structure of claim 39 wherein said gate electrode comprises a refractory metal.

41. The structure of claim 39 wherein said gate electrode comprises a member of the group consisting of W, WN, WSi , and combinations thereof.

42. The structure of claim 39 wherein said gate insulator structure further comprises a third layer.

43. The structure of claim 42 wherein said third layer comprises compounds comprising gallium and oxygen.

44. The structure of claim 43 wherein compounds of said third layer comprising gallium and oxygen further comprise a rare earth element.

45. The structure of claim 44 wherein a composition of said third layer varies monotonically with depth in said third layer.

46. The structure of claim 43 wherein said gate insulator structure further comprises a

fourth layer.

47. The structure of claim 43 wherein said fourth layer comprises compounds comprising gallium and oxygen.

48. The structure of claim 47 wherein compounds of said fourth layer comprising gallium and oxygen further comprise a rare earth element.

49. The structure of claim 39 wherein said first layer is adjacent and in contact with said upper surface.

50. The structure of claim 39 further comprising source and drain contacts.

51. The structure of claim 39 wherein said source and drain contacts are rapid thermal annealed in UHV.

52. The structure of claim 39 wherein said gate insulator structure passivates said upper surface.

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53. A method for forming an enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

54. The method of claim 53 comprising rapid thermal annealing said structure in UHV.

55. The method of claim 54 wherein said rapid thermal annealing comprising annealing at between 700 and 900 degrees Centigrade.